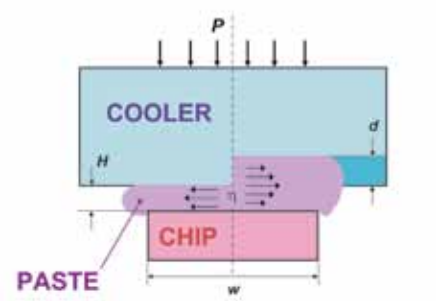
Novel Approach Offers Significant Improvements in Thermal Interface Material Performance®

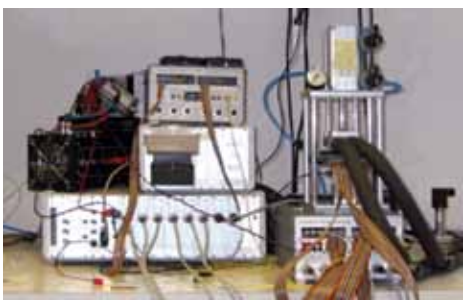
T3Ster®

Design Challenge

The performance of Thermal Interface Materials (TIMs) has become a thermal "bottleneck" between a high performance chip package and its heat sink.Traditionally TIMs are characterized experimentally according to the ASTM standard D 5470-95, but this does not measure the material thickness and uses much higher clamping pressures than found in electronics applications. Hence the method does not provide meaningful data, so the actual performance of the TIM can be quite different from that stated in the vendor's data sheet.

TIMs come in a variety of forms - thermal pastes, greases, phase change materials, adhesives and even metal interfaces. The advantages of thermal pastes are their low cost, ease of assembly and re-workability, making them much more suitable for volume electronics. The disadvantages are their relatively large thermal resistance and susceptibility to voiding and dry-out, ruling them out when performance or reliability are of paramount importance.





Solution and Benefits

Bruno Michel and his Advanced Thermal Packaging team at the IBM Zurich Research Laboratory speculated that voiding could be reduced by minimizing pressure gradients in the paste during thermal cycling. The idea the team hit on was to develop a novel type of interface structure using Hierarchically Nested Channels (HNCs) that would allow the paste to flow more easily during thermal cycling.

Naturally, the researchers wanted to test their hypothesis under conditions that closely mimic an actual processor, interface and heat sink. Having built a suitable experimental setup, the team chose the MicReD *T3Ster* equipment to perform the thermal measurements.

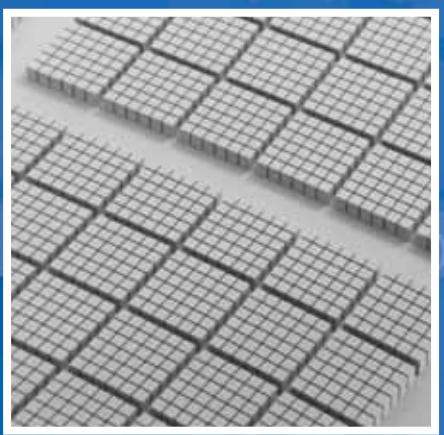
T3Ster's very high fidelity temperature vs. time measurements yield detailed information on the heat flow path from the silicon to the heat sink, and can be used under typical operating conditions. The associated analysis software extracts the thermal resistances and capacitances, there by allowing the thermal resistance of the TIM to be determined.

HNCs are so successful at reducing the flow resistance of the TIM that voiding caused by paste flow during thermal cycling is alleviated. The researchers also found that the HNC interfaces reduced the thermal resistances between the chip, heat spreader and heat sink, facilitating faster assembly with fewer voids. They concluded that HNCs meet the urgent need of the computer industry for improved thermal interface performance and will soon result in products with better performance and reliability.

Customer Testimonial

"To reliably measure the interface resistance we needed a transient measuring method. We chose the T3Ster because of its compactness and ease of use, allowing us to improve data acquisition and processing of the transient thermal data. We were able to improve the accuracy of TIM measurements and measure the contribution of the different components – the heater chip, thermal interface, cooling cap, second interface, and heat sink."

Dr. Bruno Michel
- Advanced Thermal Packaging Manager
IBM Zurich Research Laboratory,
Switzerland



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